Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **GND**
2. **SHUTDOWN**
3. **OUTPUT**
4. **INPUT**
5. **ADJUST**

**.45”**

**MASK**

**REF**

**1**

**2**

**3**

**3**

**3**

**3**

**5**

**4**

**4**

**4**

**4**

**.176”**

**Top Material: Al**

**Backside Material: Ti/Ni/Ag**

**Bond Pad Size: .004 x .004”**

**Backside Potential: GND**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .045” X .176” DATE: 9/23/20**

**MFG: MICREL THICKNESS .014” P/N: MIC2941A**

**DG 10.1.2**

#### Rev B, 7/1